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| 09/808,676 | 03/15/2001 | Alain R. Comeau | 1820-2001 | 5150 |

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| ART UNIT | PAPER NUMBER |
|---|---|
| 2836 | |

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Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/808,676 | COMEAU, ALAIN R. | |
| | Examiner | Art Unit | |
| | Zeev Kitov | 2836 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *22 October 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1 -24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 -24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 3 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

## DETAILED ACTION

### *Objection*

1. Claims 1 and 9 are objected to due to following statements. Claim 9 states: "thereby limiting the leakage current of each of said transistors to a sub-threshold level even as said source voltage increases". According to this statement, an increase in the transistor current for bypassing an ESD transient cannot occur. The same conclusion can be drawn from a statement in Claim 1: "where the leakage current of said transistor is reduced to a sub-threshold level while an increasing source voltage applied at said source terminal reduces the gate-to-source voltage and reduces its threshold voltage". However, Claim 18 includes a limitation that overcomes this deficiency stating: "wherein a leakage current of said input protection transistors is controlled to a sub-threshold level over a range of voltages applied to each source terminal of said input protection transistors" (emphasis added). In other words, the transistor current is kept at subthreshold level only for voltages applied to the source terminals. Implicitly for voltages beyond the source terminals values the transistor current may increase, thus fulfilling its protection function. The same or similar limitations should be added to Claims 1 and 9. For purpose of examination it was assumed that the Claims 1 and 9 have the same limitations as the one in Claim 18.

Claims 4, 13, 24 are objected due to use of symbol "Vss". Even though it is common in EE sources to indicate the lowest potential supply terminal as Vss, its presence in the claim results in some uncertainty. A more definitive limitation should be

used. For purpose of examination it was assumed that Vss stands for the lowest potential supply terminal.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

2. Claims 6 and 15 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Following statements make the claims indefinite: "the resulting leakage current from said source voltage is approximately $10^{-14}$ A/μm". The current is defined as amount of charge per cross sectional area (per squared value of length). Citation of current value in amperes per units of length makes the claims indefinite. Accordingly meats and bounds of the claim cannot be determined. The claim has not been treated with regard to prior art.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 5 and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by Smith (US 5,903,419). Smith discloses an ESD protection having a transistor with gate,

source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/O PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 – 29, col. 4, lines 1 –5, col. 9, lines 25 –35).

Regarding Claim 5, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2).

Regarding Claim 8, discloses a PMOS transistor (element 204in Fig. 2).

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 7 and 2 - 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Smith in a view of A. Sedra and K. Smith textbook "Microelectronic Circuits". As was stated above, Smith discloses all the elements of Claim 1. However, regarding Claim 7, it does not disclose the NMOS transistor. According to the Microelectronic

Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

Regarding Claims 2 - 4, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the ground, or Vss (the lowest potential) voltage for NMOS transistor. Therefore, for the equivalent PMOS transistor the reference potential is equal Vdd volts, rather than 0 volts.

5. Claims 9, 14, 17, 18 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. (US 5,751,507) a view of Smith.

Regarding Claims 9 and 18, Watt et al. discloses an ESD protection solution for a plurality of low operating voltage devices having a plurality of input terminals (input pads 1, 2, ...., N in Fig. 2). Each input has its own ESD protection (elements D1 and D3 in Fig. 2).

However, he does not disclose a low leakage current solution for ESD protection devices. Smith discloses an ESD protection having a transistor with gate, source, drain and substrate terminals (element 204 in Fig. 2), an input terminal coupled to the source terminal of the transistor (I/O PAD 14 in Fig. 2), a reference point coupled to the gate and substrate terminals of the transistor (Vdd in Fig. 2), and an output signal terminal

coupled to the drain terminal of the transistor (base of transistor 202 is coupled to the drain of transistor 204 in Fig. 2). Due to a diode (element 206 in Fig. 2), a gate to substrate voltage is always positive, which moves the PMOS transistor into sub-threshold regime. Increase of the transistor source voltage reduces the source-to-gate threshold. One of the goals of the invention in the reference is a reduction of a leak current (col. 2, lines 20 – 29, col. 4, lines 1 –5, col. 9, lines 25 –35). Both patents have the same problem solving area, namely providing an efficient ESD protection for integrated circuits. Therefore it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the plurality of transistors according to Smith protecting each of the inputs of the Watt et al. circuit, because as well known in the art and stressed by Smith (col. 2, lines 20 – 29), the leakage current presents a problem in many electronic circuits, especially in a view that they increase with a temperature.

Regarding Claim 14, Smith discloses the device having the source voltage of a few hundreds millivolts (a voltage drop across diode 206 in Fig. 2).

Regarding Claim 17 and 20, discloses a PMOS transistor (element 204 in Fig. 2).

6. Claims 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in view of Smith and further in a view of Ker et al. article "Capacitor-Coupled ESD Protection Circuit for Deep-Submicron Low-Voltage CMOS ASIC". As was stated above, Watt et al. and Smith disclose all the elements of Claim 9.However, regarding Claim 10, they do not disclose the solution according to teachings of Watt et al. and Smith being

used for protection of the low voltage CMOS circuit. Ker et al. discloses an ESD protection for the low voltage CMOS circuit. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used the solution according to teachings of Watt et al. and Smith for protection of the low voltage CMOS circuit, because as Ker et al. state (see Operating Principles pages 310 – 311), the submicron low voltage CMOS circuits more than other circuits need the ESD protection.

7. Claims 16, 19,11 – 13 and 22 - 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Watt et al. in a view of Smith and further in a view of A. Sedra and K. Smith textbook "Microelectronic Circuits". As was stated above, Watt et al. and Smith disclose all the elements of Claim 9. However, regarding Claims 16 and 19, they do not disclose the NMOS transistor. According to the Microelectronic Circuits textbook (pages 3442 -343), the NMOS and PMOS transistors are equivalents and are interchangeable. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have used NMOS transistor as equivalent replacement for PMOS transistor, because as the textbook states (pages 243 -343), they are equivalents and interchangeable. Selection of particular type of transistor is a designer decision, which is far from being an inventive step.

Regarding Claims 11 – 13 and 22 – 24, Smith discloses the reference point (element Vdd in Fig. 2), which for PMOS transistor plays the same role as the

ground, or Vss voltage for NMOS transistor. Therefore the reference potential is equal Vdd volts, rather than 0 volts.

***Conclusion***

The prior art made of record not relied upon is considered pertinent to applicant's disclosure: US 6,144,542, US 5,959,488, 6,249,410, 5,852,541.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zeev Kitov whose telephone number is (703) 305-0759. The examiner can normally be reached on 8:00 – 4:30. If attempts to reach examiner by telephone are unsuccessful, the examiner's supervisor, Brian Sircus can be reached on (703) 308-3119. The fax phone numbers for organization where this application or proceedings is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Z.K.
04/14/2003

GREGORY J. TOATLEY, JR.
PRIMARY EXAMINER